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W. Lawson
7/27/02

ATTORNEY'S DOCKET NO: **A1998017 (formerly A0521/7153)**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: FRINK, Craig
Serial No: 09/054,933
Filed: April 3, 1998
For: METHOD AND APPARATUS FOR ACCESSING VIDEO DATA IN MEMORY ACROSS FLOW-CONTROLLED INTERCONNECTS

Examiner: K. O. Bui
Art Unit: 2611

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, Washington, D.C. 20231, on July 15, 2002.

Peter J. Gordon, Reg. No. 35,164

Commissioner for Patents
Washington, D.C. 20231

REPLY

Sir:

In reply to the Office Action of February 15, 2002, and in view of the following remarks, reconsideration is requested. Claims 1-10 remain in the application of which claims 1, 2, 3, 6, 9 and 10 are independent.

Rejection Under 35 U.S.C. §102

Claims 1-10 were rejected under 35 U.S.C. §102 in view of U.S. Patent 6,018,765 ("Durana").

Independent claims 1, 2, 3, 6, 9 and 10 all recite systems having an interface (either an output or input interface) that include data, a valid data signal that indicates if the data includes valid video data, and a command valid data signal that indicates if the data includes valid command data. *One of* the valid data signal and valid command signal is asserted, depending on whether the data includes video data or command data.

Durana teaches a system in which Fig. 6 has analog composite video and analog audio outputs. The Examiner asserts that these outputs are the claimed data output. A programmable logic device (PLD) 222 controls transfer of digital data to multimedia processors that produce the video outputs in Fig. 6.

The Examiner asserts that "the status of data, whether it is a valid video data or not, can be determined based on their memory addresses," citing Col. 16, lines 37-66. The portion of the reference that has been cited, however, has nothing to do with indicating whether audio and video outputs of Fig. 6 are valid. The cited portion of the reference merely states that some inputs to the PLD indicate that an address on an address bus is valid. See Col. 16, lines 62-64. Such an *input* to the PLD is not a signal that is part of an interface that includes the video output of Fig. 6.

The Examiner also asserts that "the command data is a memory address at the receiver," citing Col. 5, lines 55-67. This data has nothing to do with the video outputs of Fig. 6 referenced by the Examiner.

The claim states that one of the valid data signal and valid command signal is asserted, depending on whether the data includes video data or command data. In contrast, the command data and the address inputs to the PLD have no such relationship to the video outputs in Fig. 6 in Durana.

The various portions of the Durana reference cited by the Examiner (the video outputs, the PLD address inputs and the command data) are in different and unrelated parts of the system in Durana. The cited memory addresses, video outputs and command information simply are not part of an *interface* that includes video data, a valid data signal and a valid command signal as claimed. Accordingly, the rejection of claims 1, 2, 3, 6, 9 and 10 is traversed. The remaining claims are dependent claims that are allowable for the same reasons.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this reply, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	09/054,933	Group No.: 2611
Filed:	April 3, 1998	Examiner: K.O. Bui
For:	Method And Apparatus For Accessing Video Data In Memory Across Flow-Controlled Interconnects	
Inventors:	Craig Frink	
Docket No.:	A1998017 (formerly A0521/7153)	

Assistant Commissioner of Patents and Trademarks
Washington, D.C. 20231

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT BEFORE MAILING DATE OF EITHER A FINAL ACTION OR NOTICE OF ALLOWANCE (37 CFR § 1.97 (c))

Transmitted herewith for filing in the above-entitled patent application is a PTO Form SB/08A/B and copies of references cited. The information disclosure statement is being filed *before* the mailing of either a final action under § 1.113, or a notice of allowance under § 1.311, whichever occurs first.

Applicant hereby requests consideration of this information disclosure statement.

Applicant submits the fee set forth in § 1.17(p). Please charge **Deposit Account No. 50-0876** the amount of **$180.00** fee. The Commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to said Deposit Account. A duplicate copy of the sheet in enclosed.

Dated: July 15, 2002

Respectfully submitted,

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I hereby certify that this correspondence is, on the date shown below, being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner of Patents, Washington, D.C. 20231.

Dated: July 15, 2002

Peter J. Gordon
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